

Compal Confidential

ZAUSA Schematics Document

AMD "Kabini" Platform

AMD 25W APU With Jaguar Core and Integrated Yangtze FCH + ATI Sun Pro S3

LA-A331P REV: 0.1

2013-02-04
www.rosefix.com

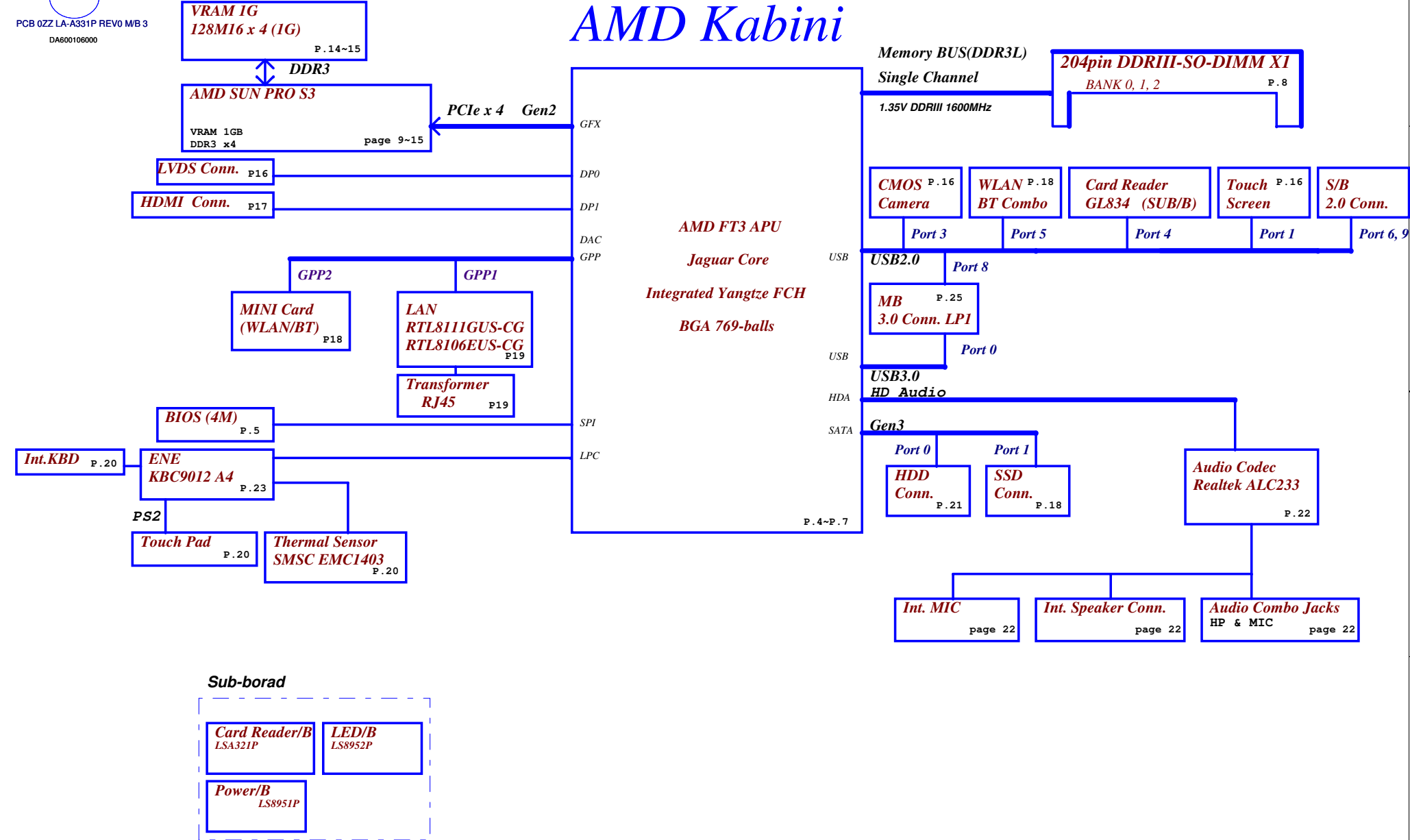
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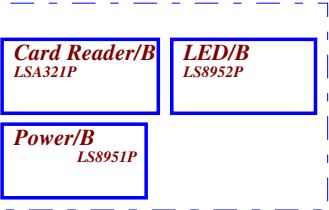
Model Name : ZAUSA



AMD Kabini



Sub-borad



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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+RTC_APU	RTC power	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+0.95VALW	0.95V always on power rail	ON	ON	ON
+1.35V	1.35V power rail for APU and DDR	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+0.95VS	0.95V switched power rail	ON	OFF	OFF
+0.675VS	0.675V switched power rail for DDR terminator	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	PX	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	PX	OFF	OFF
+3VS_VGA	3.3V switched power rail for VGA	PX	OFF	OFF
+1.8VS_VGA	1.8V switched power rail for VGA	PX	OFF	OFF
+1.5VS_VGA	1.5V switched power rail for VGA	PX	OFF	OFF
+0.95VS_VGA	0.95V switched power rail for VGA	PX	OFF	OFF

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	FCH	APU	RTD2132
SMB_EC_CK1 SMB_EC_DA1 +3VALW	KB9012	X	V	X	X	X	X	X	X	X
APU_SCLK0 APU_SDAT0 +3VS	APU	X	X	X	V	V	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2 +3VS	KB9012	V	X	X	X	X	V	X	V	X

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	Thermal Sensor	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			VGA Internal Thermal	1000 001X b	82H

APU
SM Bus address

Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	EVT
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R1562	100K +/- 5%			
Board ID	R1564	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

APU PCIE PORT LIST

Port	Device
0	
1	LAN
2	WLAN
3	

USB Port Table

USB 2.0	USB 3.0	Port	3 External USB Port
		0	RIGHT USB
		1	Touch Screen
		2	
		3	Camera
		4	CardReader
		5	WLAN/BT Combo
		6	LEFT USB2.0
		7	
	XHCI	0	LEFT USB3.0
		1	LEFT USB2.0

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

USB OC MAPPING

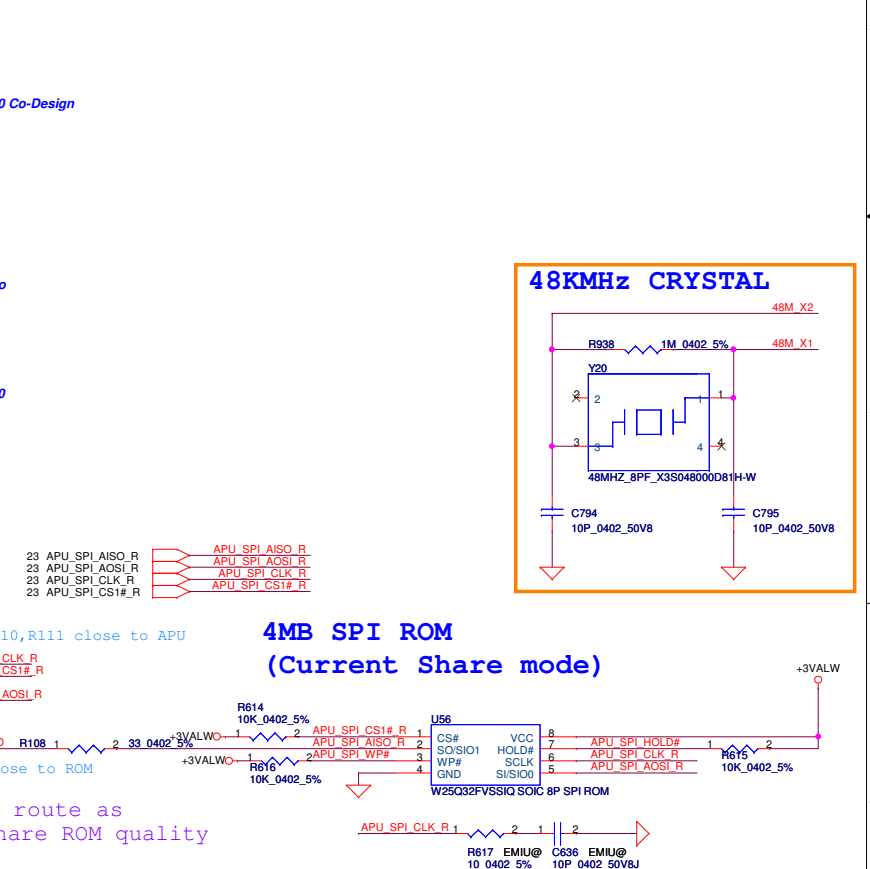
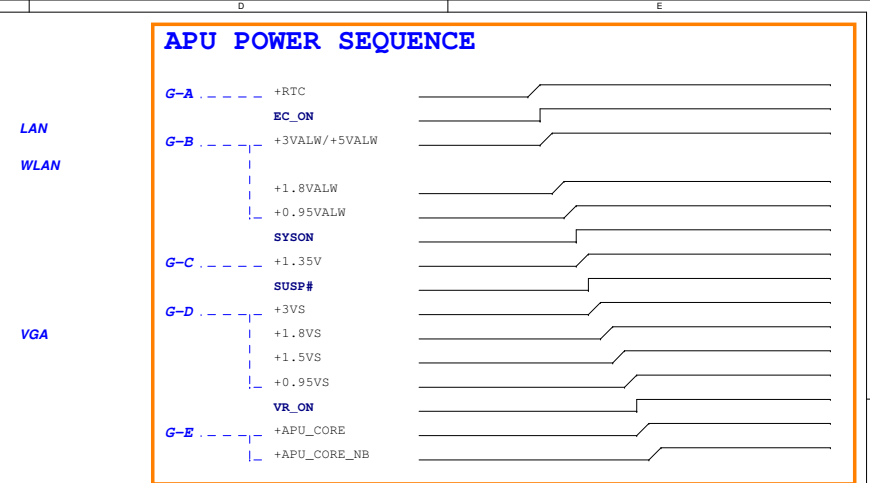
OC#	USB Port	
0	USB20 port0	
1	USB20 port1,2,8,9	USB30 port0,1
2		
3		

43190S38L01: EMIP@/ESDP@/SWR@/8106@/TS@/UMA@/43L01@
43190S38L02: EMIP@/ESDP@/SWR@/8106@/TS@/PX@/43L02@
43190S38L03: EMIP@/ESDP@/SWR@/8106@/TS@/PX@/43L03@
43190S38L04: EMIP@/ESDP@/SWR@/8106@/TS@/PX@/43L04@

BOM Structure Table

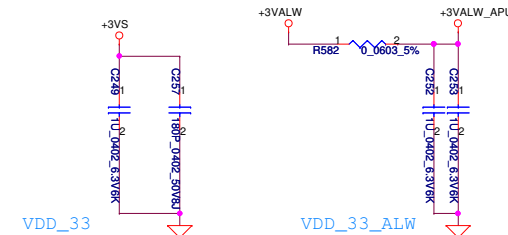
BOM Structure	BTO Item
43L01@	X4-5110 BGA APU
43L02@	X2-3450 BGA APU
43L03@	E1-2210 BGA APU
43L04@	X4-4110 BGA APU
ME@	ME part
SWR@	LAN Switching mode
LDO@	LAN LDO mode
GAS@	Gastube
PX@	Common VGA circuit
TS@	Touch Screen
EMIP@	EMI pop component
EMIU@	EMI Un pop component
ESDP@	ESD pop component
ESDU@	ESD Un pop component
X76@	VRAM
VRAM1@	Samsung 128Mbx16 K4W2G1646E-BC1A
VRAM2@	Hynix 128Mbx16 H5TC2G63FFR-11C
VRAM3@	Micron 126Mbx16 MT41J128M16JT-093G:K
8111@	Realtek RTL8111GUS-CG (Giga LAN)
8106@	Realtek RTL8106EUS-CG (10/100M)
@	Unpop

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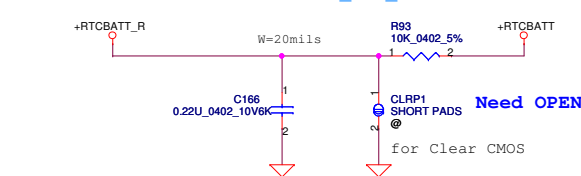


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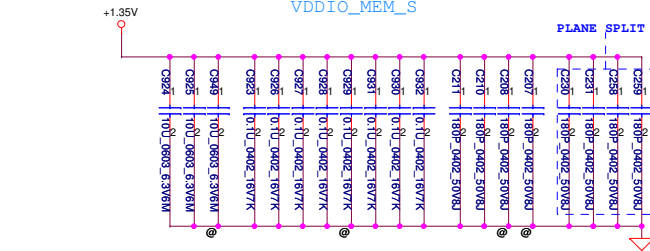
+3VALW/+3VS OF APU



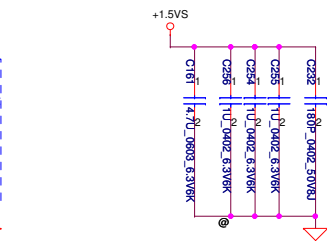
RTC OF APU



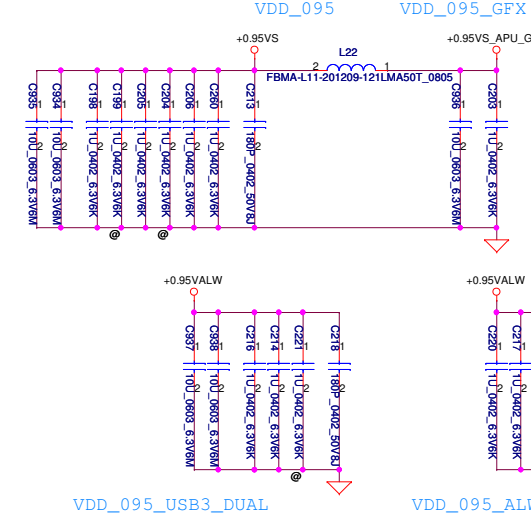
+1.35V OF APU



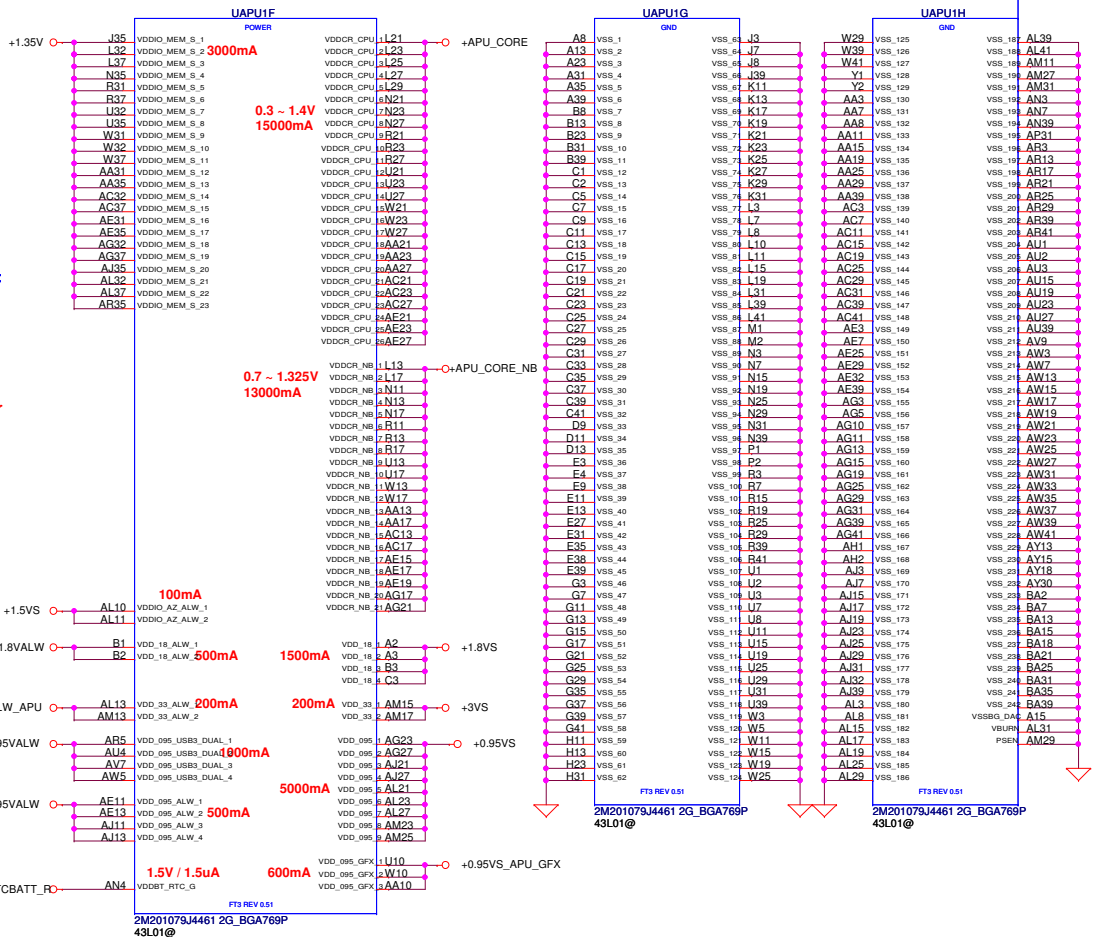
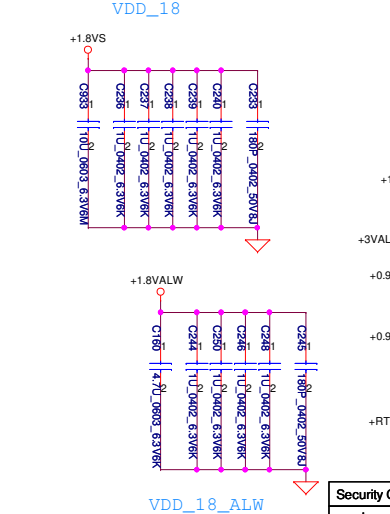
VDDIO_AZ_ALW (Could be S0 or S5 power rail)



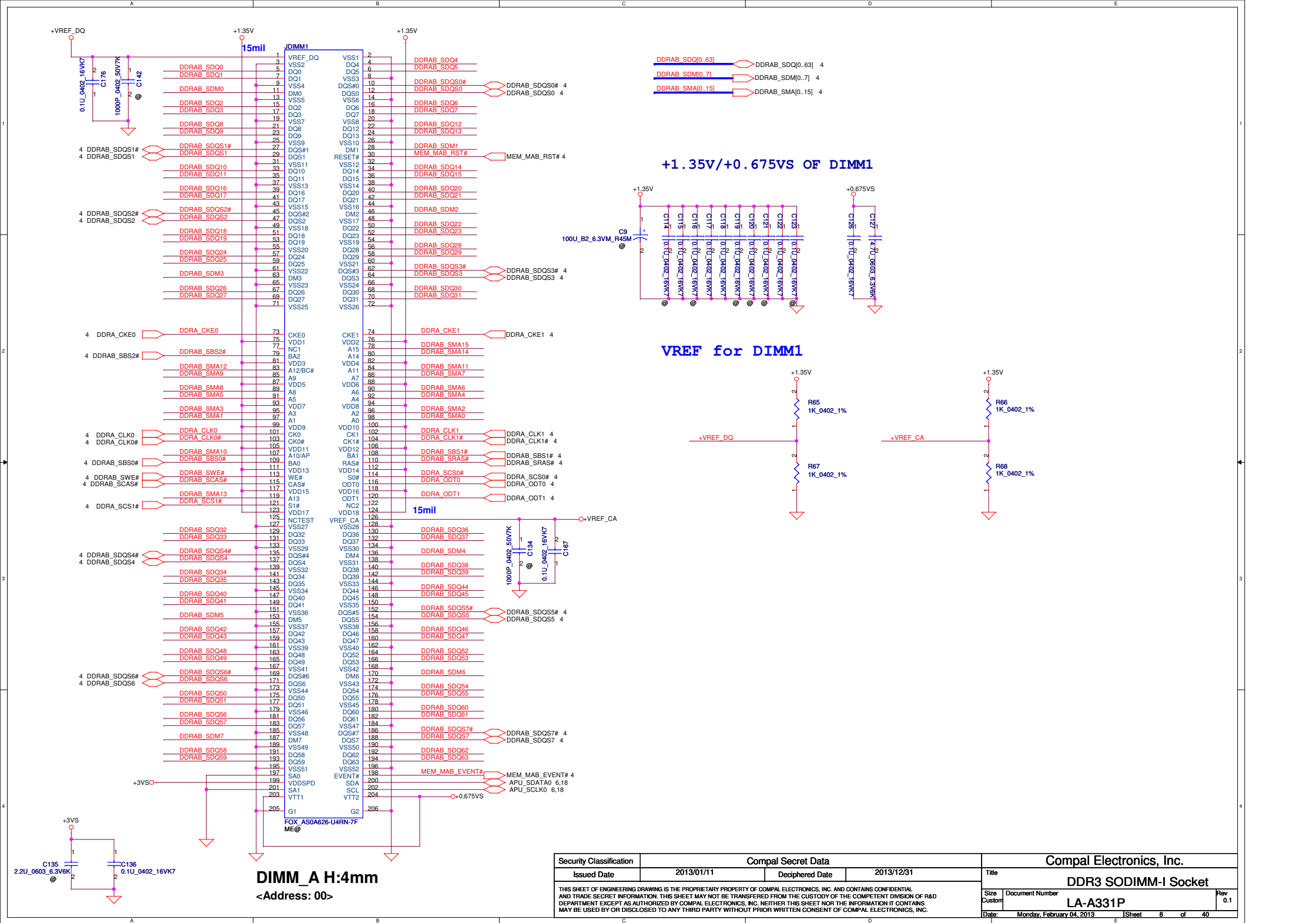
+0.95VALW/+0.95VS OF APU



+1.8VALW/+1.8VS OF APU

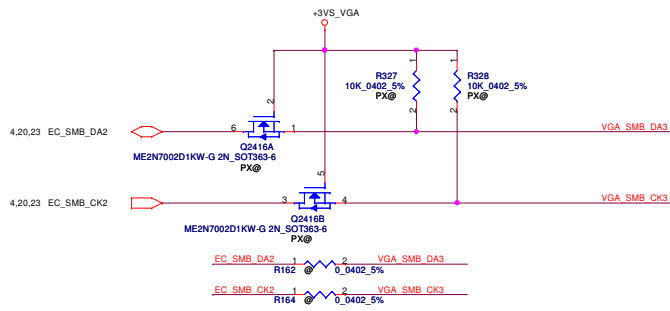


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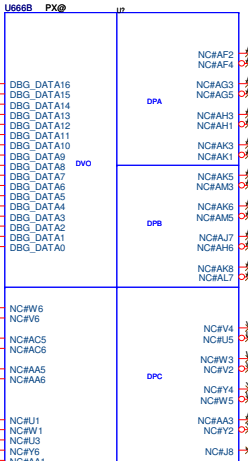




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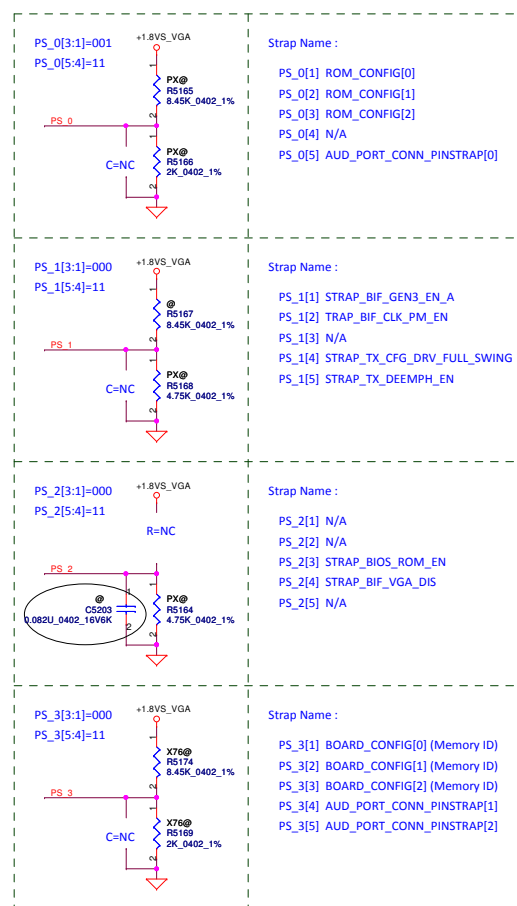
- T201 DBQ_DATA16
- T202 DBQ_DATA15
- T203 DBQ_DATA14
- T204 DBQ_DATA13
- T205 DBQ_DATA12
- T206 DBQ_DATA11
- T207 DBQ_DATA10
- T208 DBQ_DATA9
- T209 DBQ_DATA8
- T210 DBQ_DATA7
- T211 DBQ_DATA6
- T212 DBQ_DATA5
- T213 DBQ_DATA4
- T214 DBQ_DATA3
- T215 DBQ_DATA2
- T216 DBQ_DATA1
- T217 DBQ_DATA0



Resistor Divider Lookup Table		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

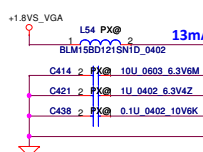
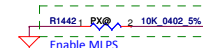
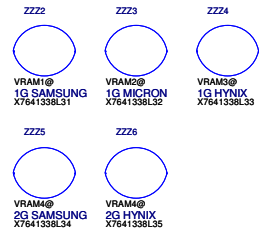
0402 1% resistors are required

Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

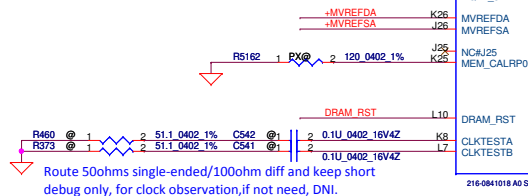


(default)

Memory ID	Memory Type	Configuration	Size	R5174	R5169	X76 P/N
000	SA000068U00	Samsung K4W2G1646E-BC1A	1GB	NC	4.75K	X7641338L31
001	SA000067500	Micron MT41J128M16JT-093G:K	1GB	8.45K	2K	X7641338L32
010	SA00006H400	Hynix H5TC2G63FFR-11C	1GB	4.53K	2K	X7641338L33
011	SA000068R00	Samsung K4W4G1646B-HC11	2GB	6.98K	4.99K	X7641338L34
100	SA000065D00	Micron MT41K256M16HA-107G:E	2GB	4.53K	4.99K	X7641338L35

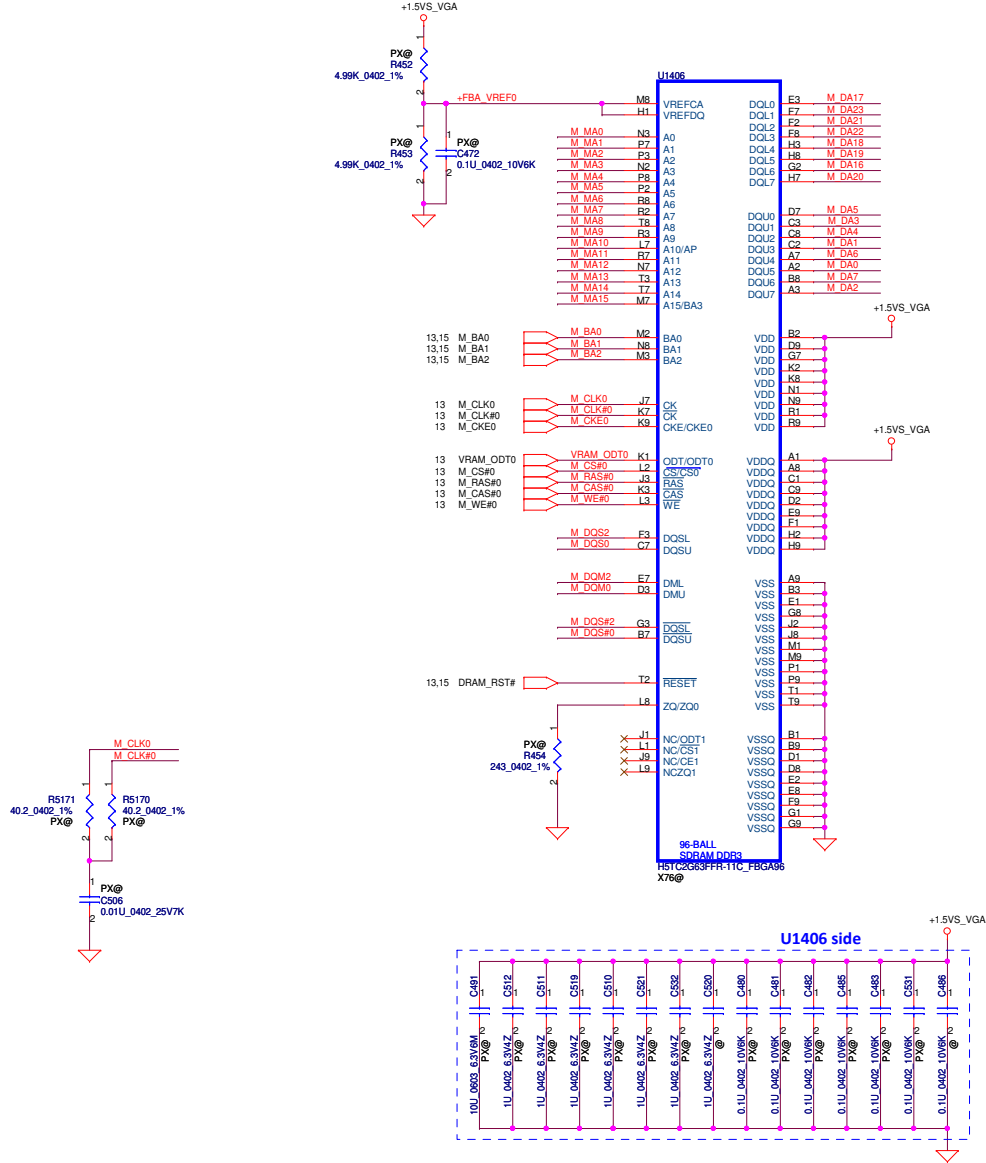


216-0841018 A0 SUN PRO '83

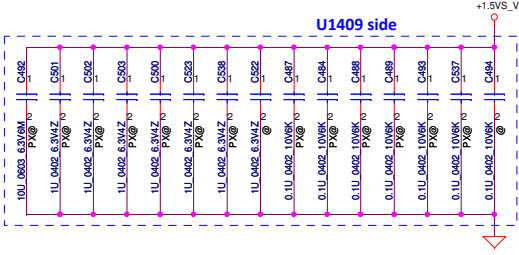
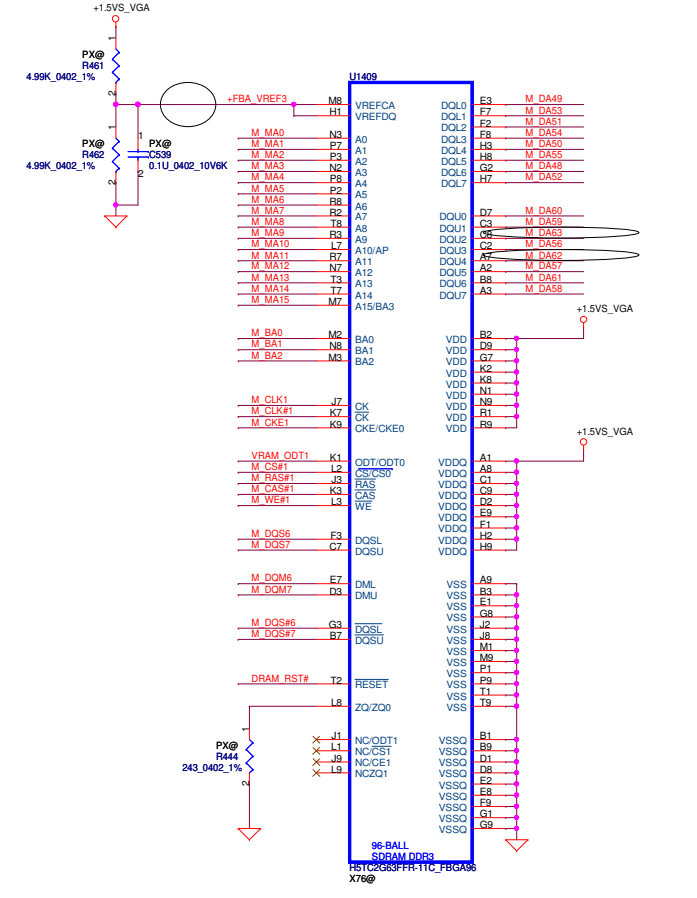
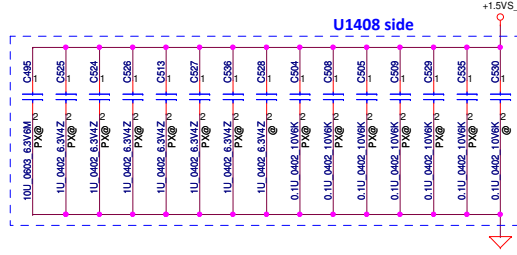
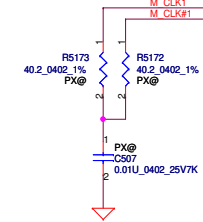
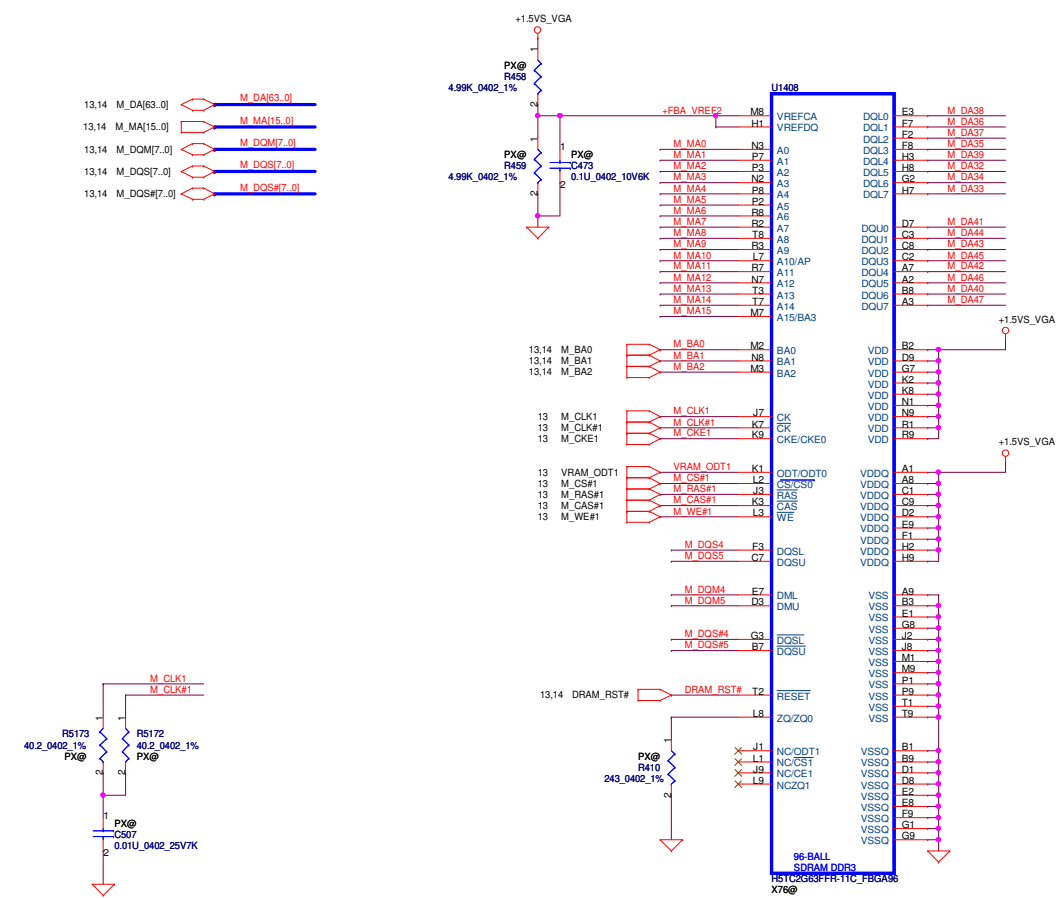


Memory Partition A - Lower 32 bits

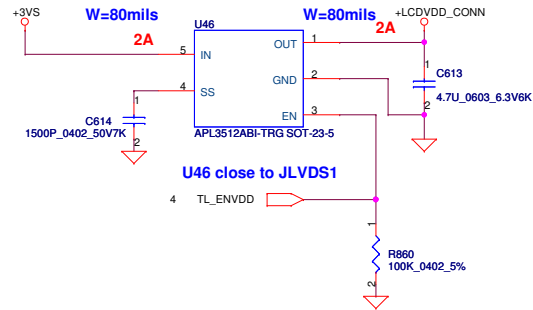
- 13,15 M_DA[63..0] M_DA[63..0]
- 13,15 M_MA[15..0] M_MA[15..0]
- 13,15 M_DQM[7..0] M_DQM[7..0]
- 13,15 M_DQS[7..0] M_DQS[7..0]
- 13,15 M_DQS[7..0] M_DQS[7..0]



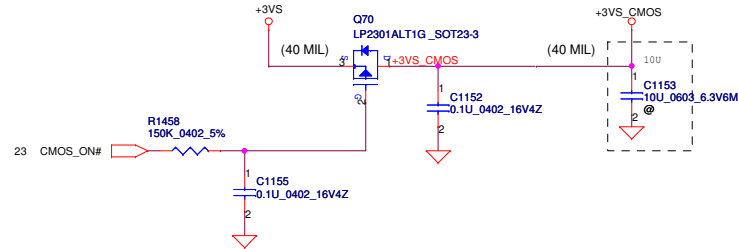
Memory Partition A - Upper 32 bits



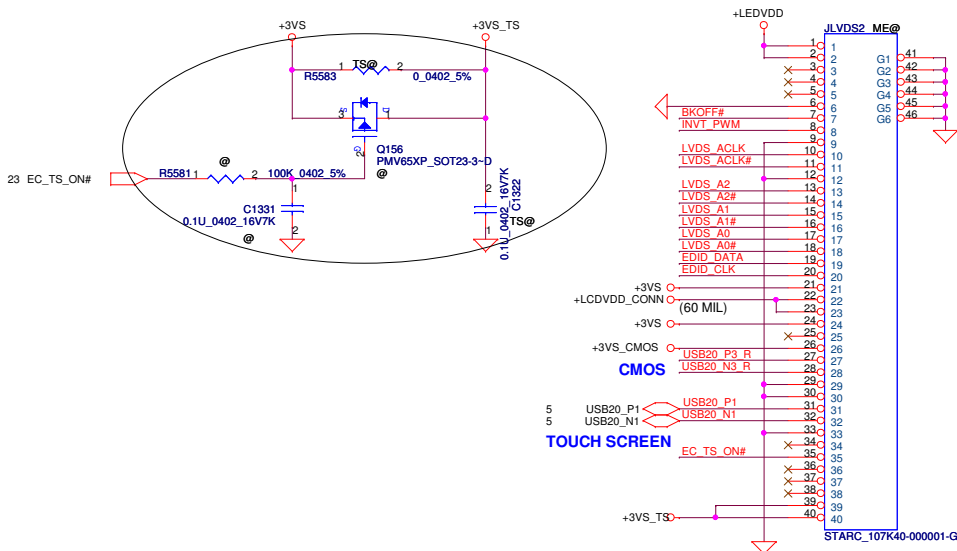
LCD POWER CIRCUIT



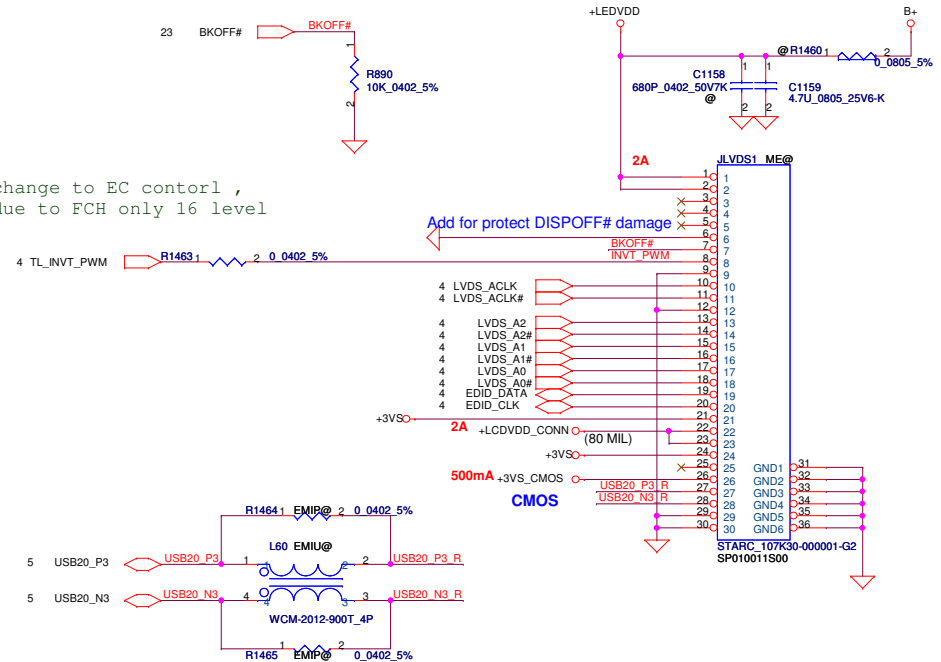
CMOS Camera



VGA LCD/PANEL BD. Conn.



change to EC control ,
due to FCH only 16 level



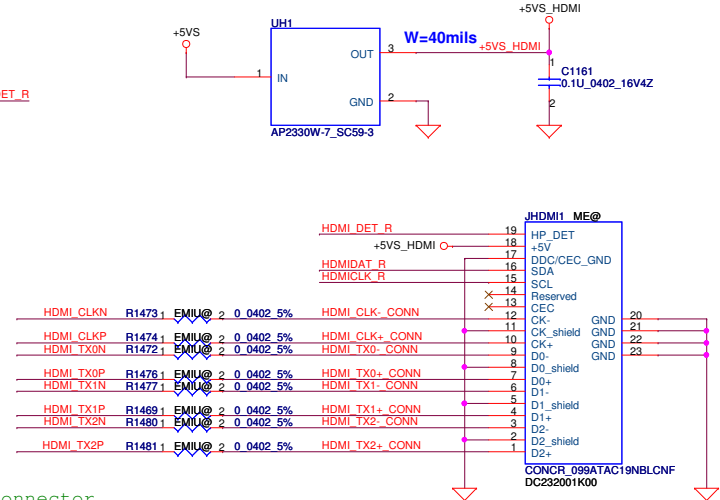
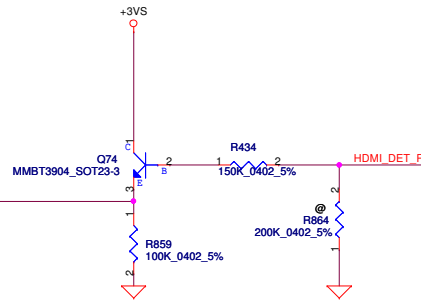
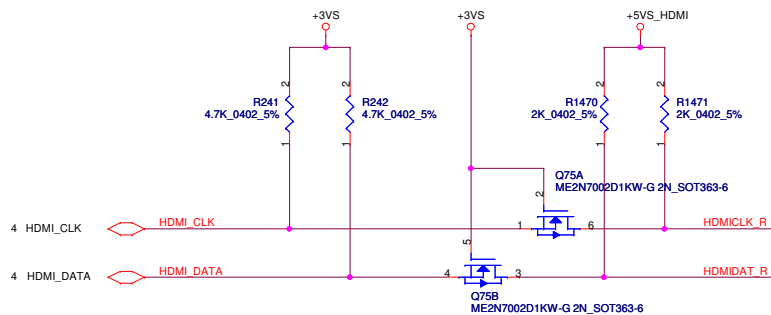
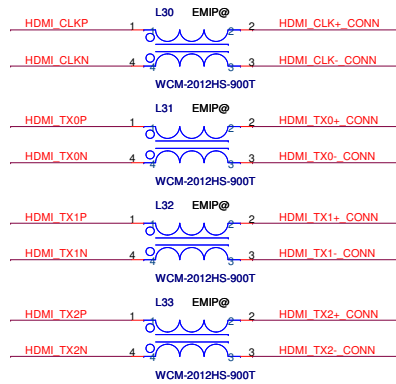
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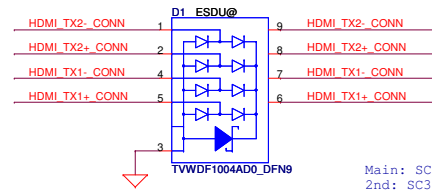
LVDS/CAMERA

Rev 0.1

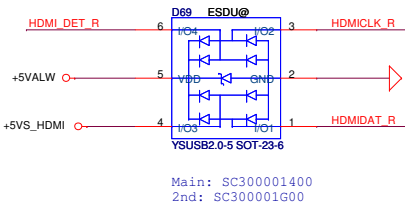
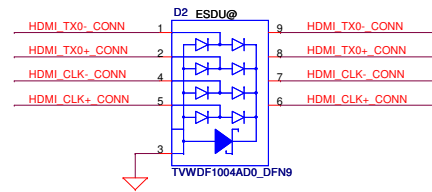
4	DP2_TXP0	DP2_TXP0	C46	1	2	0.1U	0402	16V7K	HDMI_TX2P
4	DP2_TXN0	DP2_TXN0	C47	1	2	0.1U	0402	16V7K	HDMI_TX2N
4	DP2_TXP1	DP2_TXP1	C48	1	2	0.1U	0402	16V7K	HDMI_TX1P
4	DP2_TXN1	DP2_TXN1	C55	1	2	0.1U	0402	16V7K	HDMI_TX1N
4	DP2_TXP2	DP2_TXP2	C56	1	2	0.1U	0402	16V7K	HDMI_TX0P
4	DP2_TXN2	DP2_TXN2	C68	1	2	0.1U	0402	16V7K	HDMI_TX0N
4	DP2_TXP3	DP2_TXP3	C72	1	2	0.1U	0402	16V7K	HDMI_CLKP
4	DP2_TXN3	DP2_TXN3	C74	1	2	0.1U	0402	16V7K	HDMI_CLKN



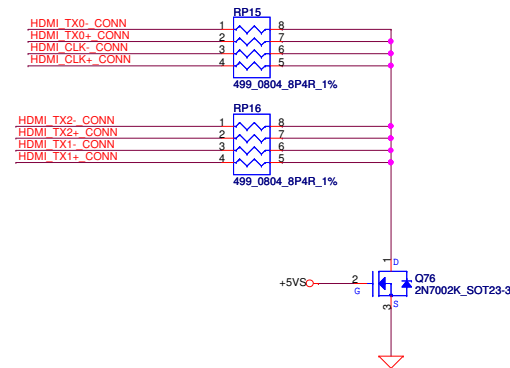
Close to HDMI connector



Main: SC300002800
2nd: SC300001Y00

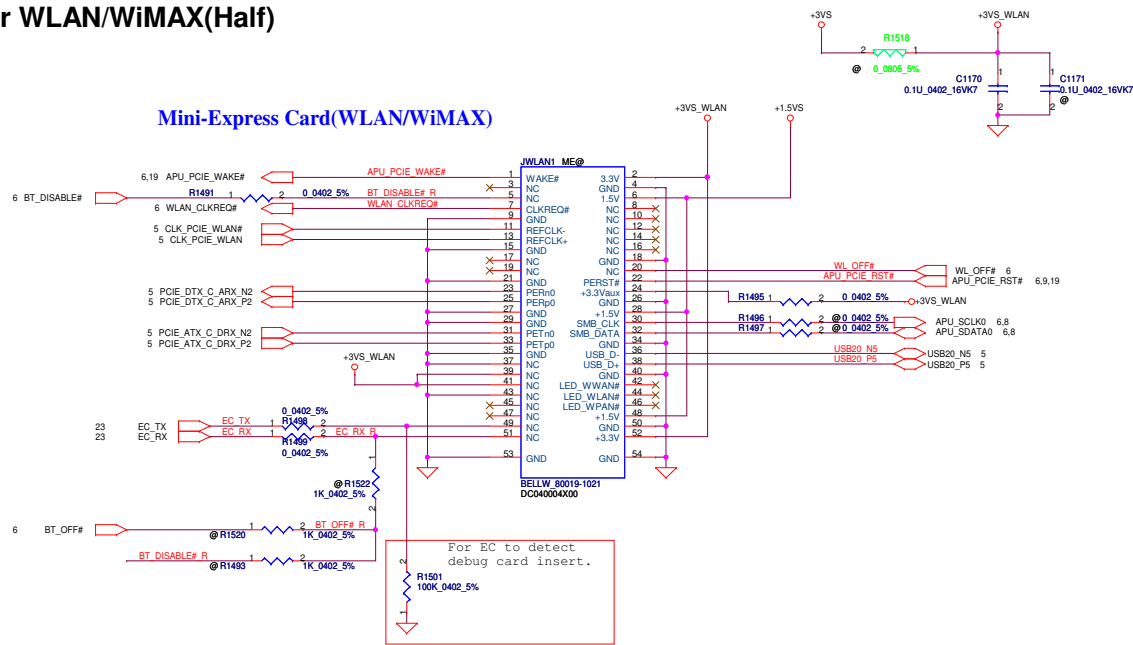


Main: SC300001400
2nd: SC300001G00

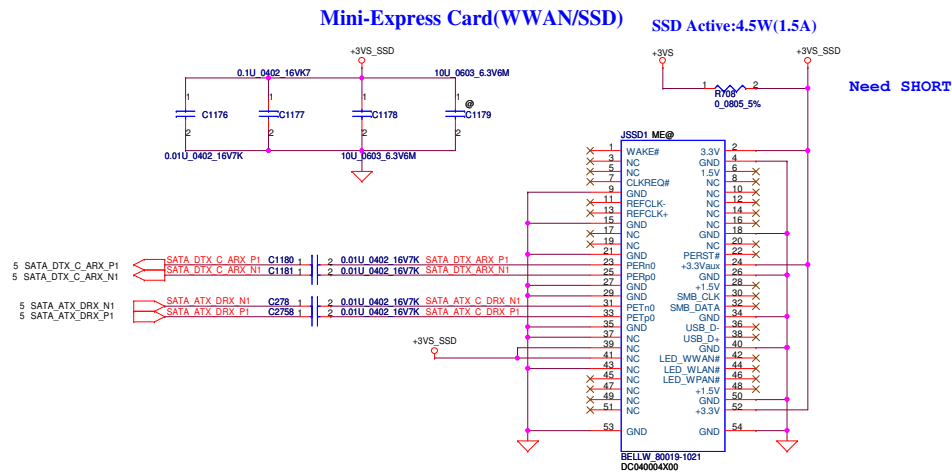


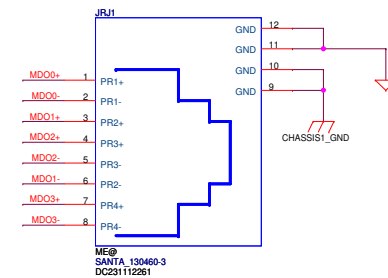
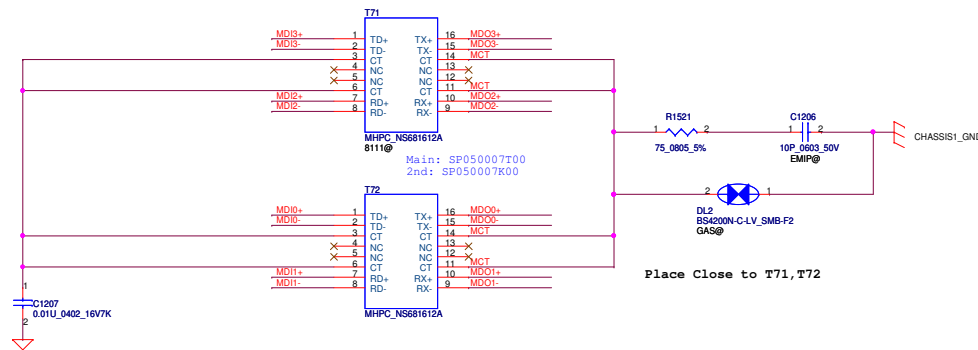
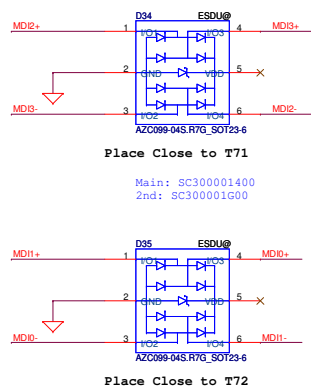
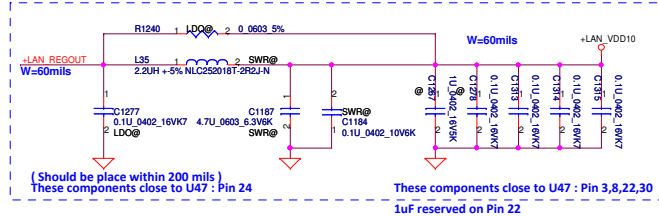
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Issued Date	2013/01/11	Deciphered Date	2013/12/31	Title	
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				Size	Document Number
				Custort	LA-A331P
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Mini-Express Card for WLAN/WiMAX(Half)



Mini-Express Card for SSD(Full)





[illegible]

The schematic diagram illustrates the connection of the TP_CLK and TP_DATA signals on the ACES_88514-00601-07 board. The signals are connected to the APU_SCLK1 and APU_SDAT1 pins of the APU module. The diagram includes components such as resistors R1830, R1831, capacitors C1302, C1303, C1304, C1305, and C1301, and connectors JTP1. The signals are also connected to the TP_CLK and TP_DATA pins of the APU module. The diagram shows the connection of the TP_CLK and TP_DATA signals to the APU_SCLK1 and APU_SDAT1 pins of the APU module. The signals are also connected to the TP_CLK and TP_DATA pins of the APU module. The diagram shows the connection of the TP_CLK and TP_DATA signals to the APU_SCLK1 and APU_SDAT1 pins of the APU module. The signals are also connected to the TP_CLK and TP_DATA pins of the APU module.

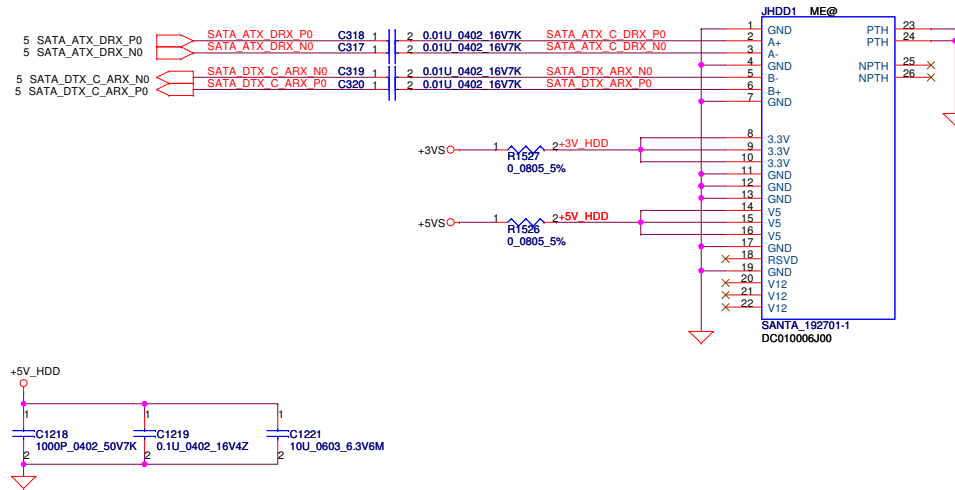
[illegible]

The diagram shows two components, C1211 and C1213, each with two pins labeled 1 and 2. C1211 is connected to REMOTE1+ (pin 1) and REMOTE1- (pin 2). C1213 is connected to REMOTE2+ (pin 1) and REMOTE2- (pin 2).

```
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"
```

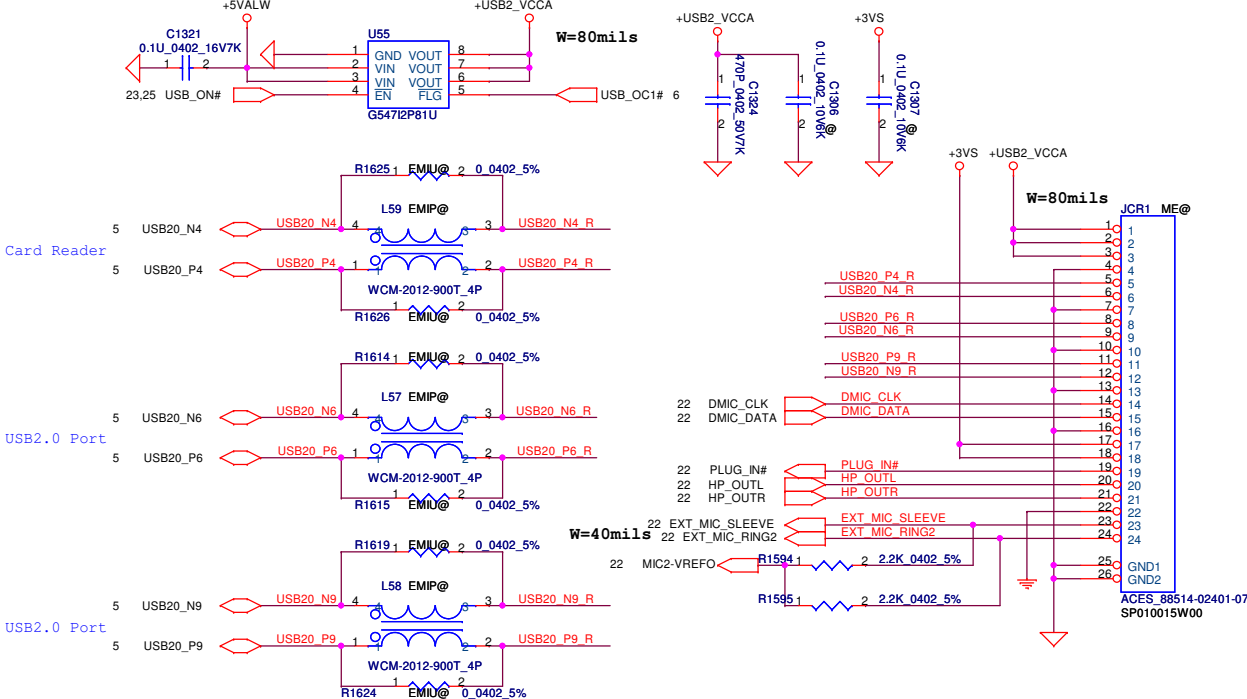
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				Size Custom	Document Number	Rev	
				LA-A331P		0.1	
Date: Monday, February 04, 2013				Sheet	20 of 40		

SATA HDD Conn.

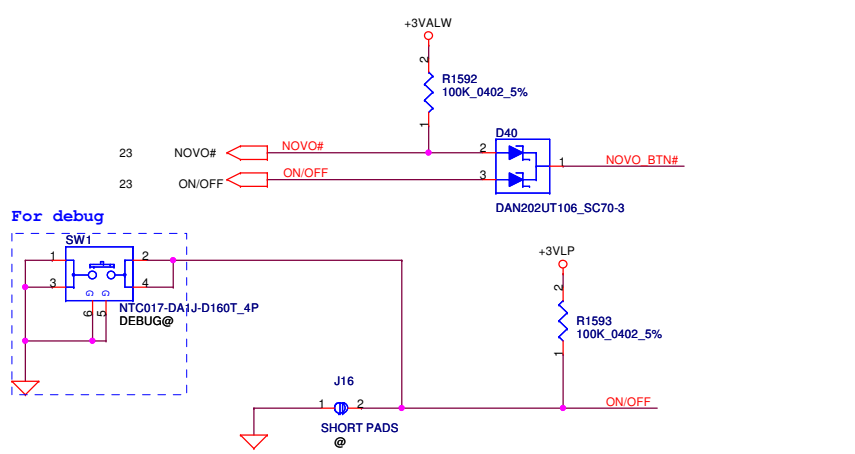
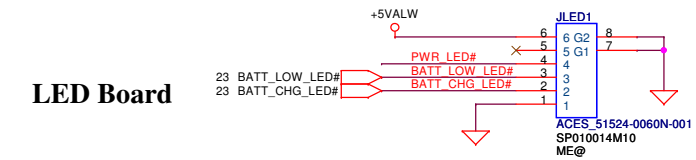


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				Custom LA-A331P	0.1
Date:				Monday, February 04, 2013	Sheet 21 of 40

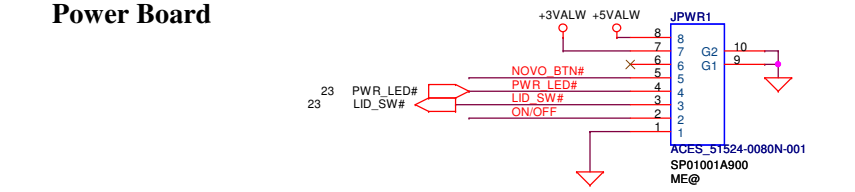
IO Board



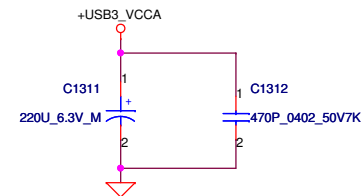
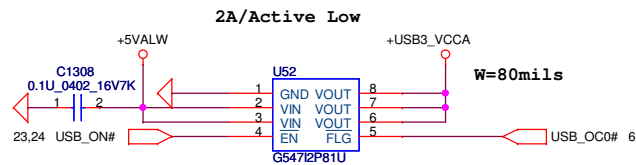
LED Board



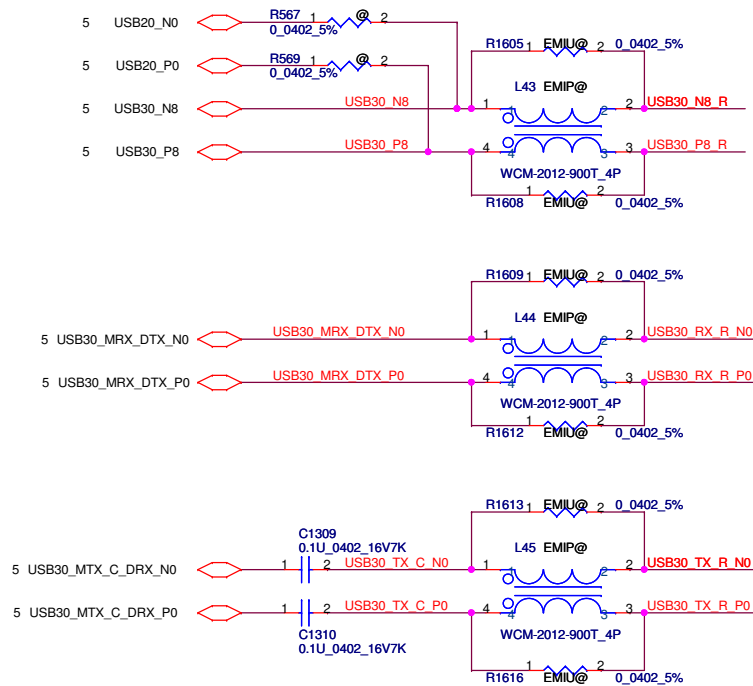
Power Board



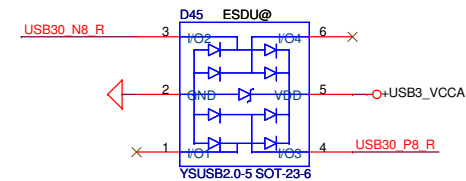
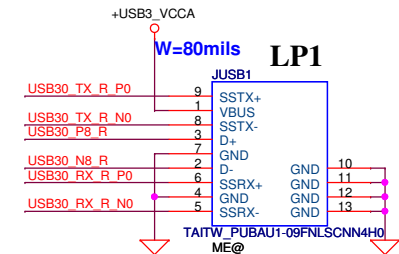
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Deciphered Date				2013/12/31				LA-A331P			
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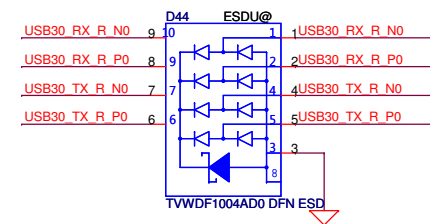
Co-Lay with USB2.0 only



Place TX AC coupling Cap (C1309,C1310). Close to connector

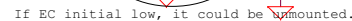
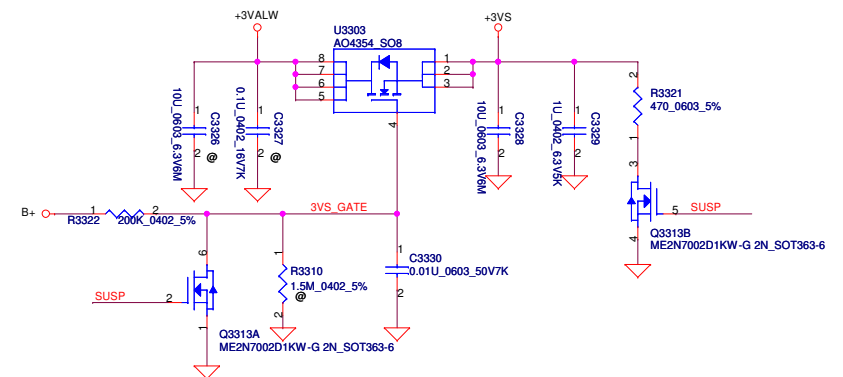
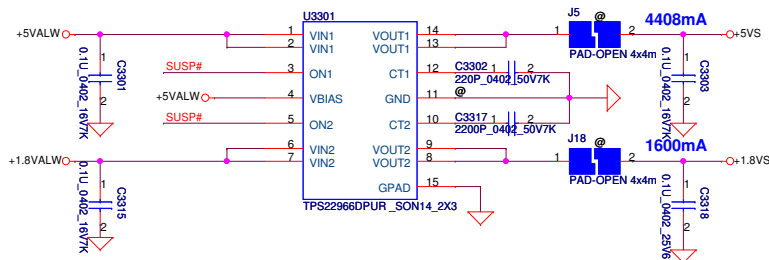


Main: SC300001400
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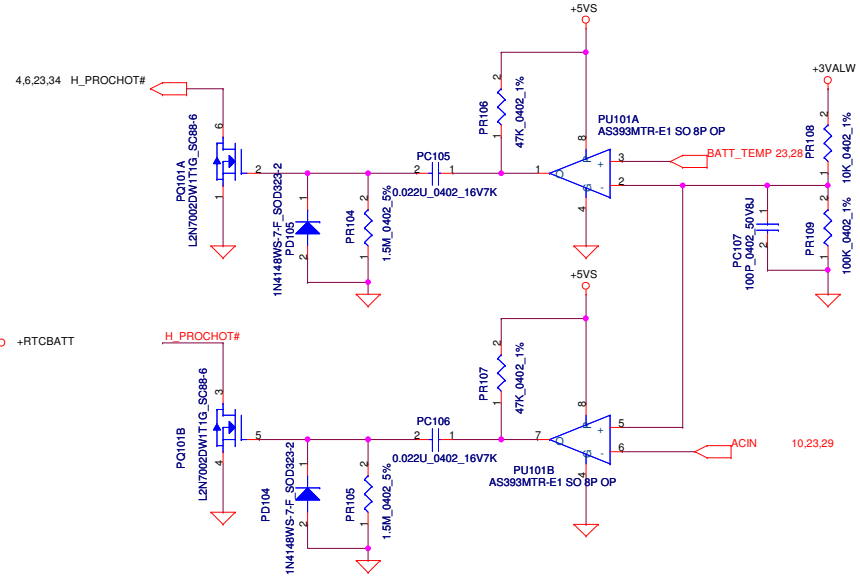
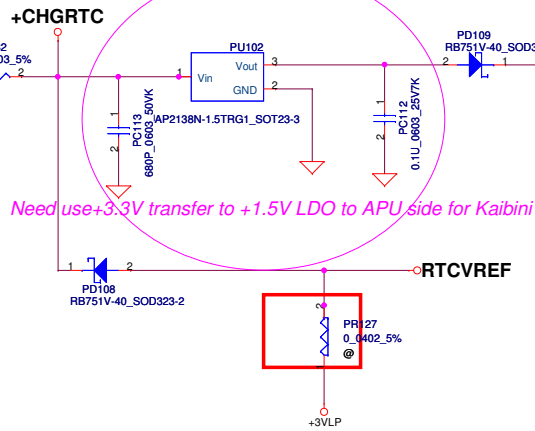
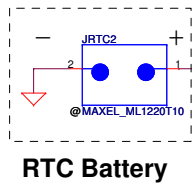
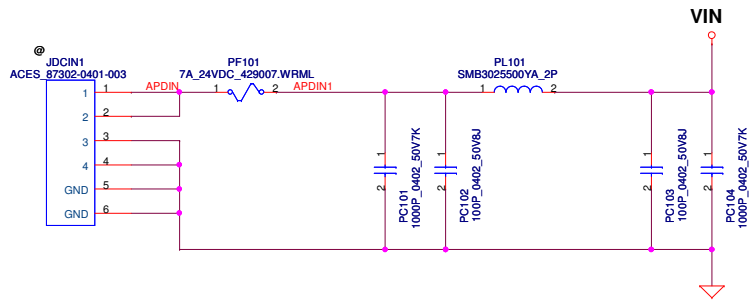


Main: SC300002800
2nd: SC300001Y00

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								Size	Document Number					Rev
								Custom	LA-A331P					0.1
Date:				Monday, February 04, 2013		Sheet		25 of 40						

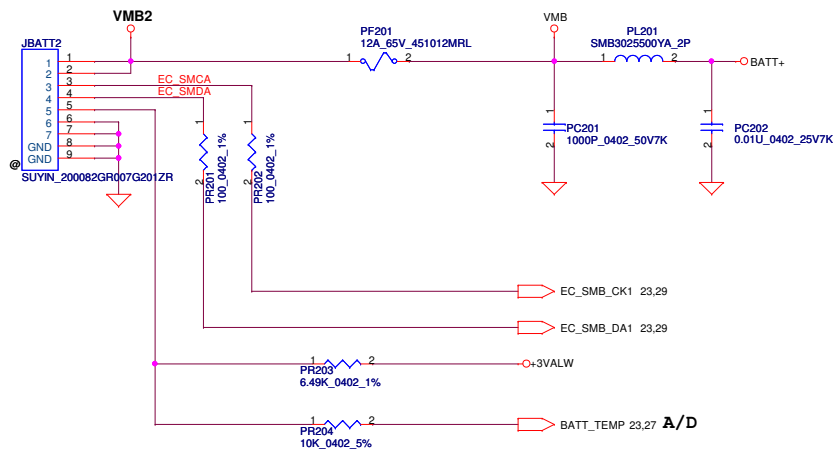


Date:	Monday, February 04, 2013	Sheet	26	of	40
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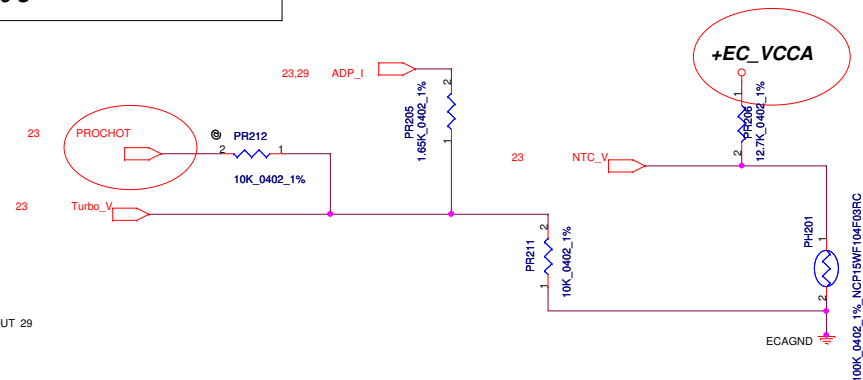
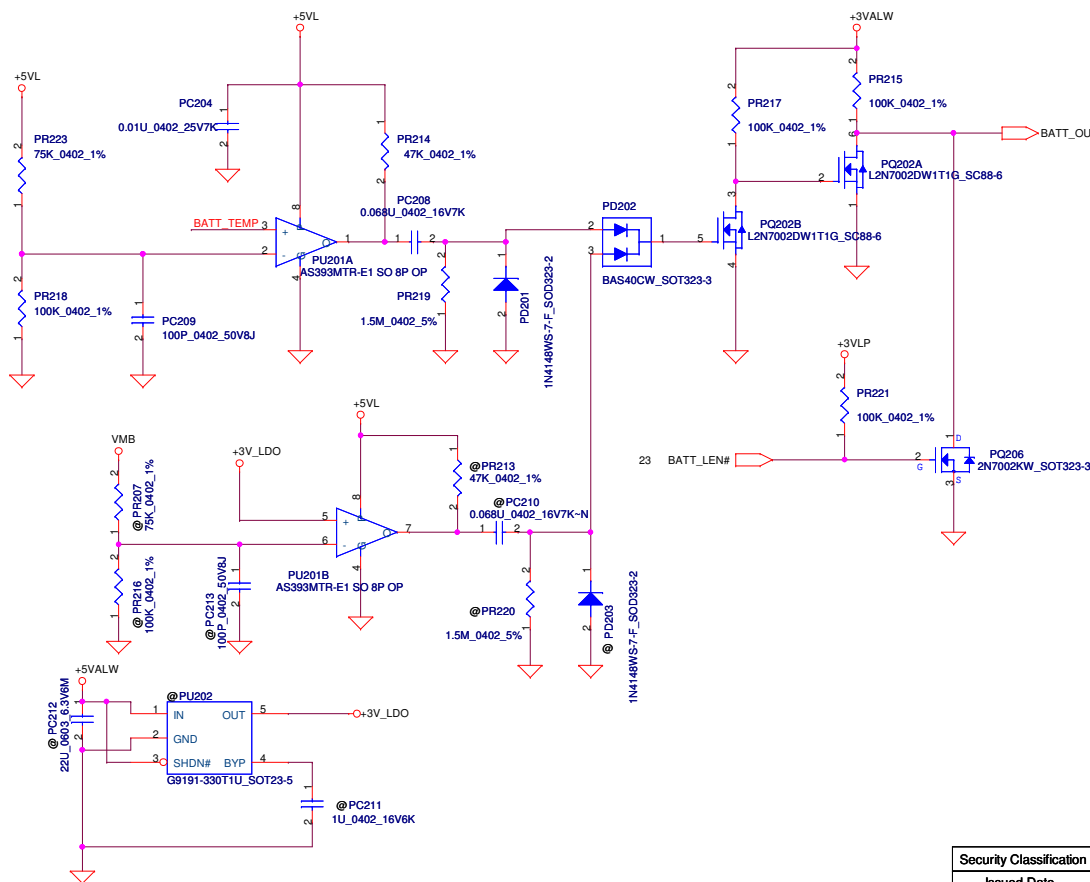
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Size	Custom	Document Number	C38-AMD KABINI Schematic	Rev	0.1
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JBATT2 Just for 14"

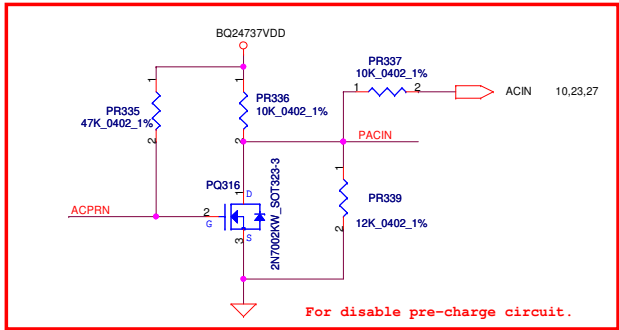


PH1 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

65W(UMA) : PR205=1.65K(SD034165180)



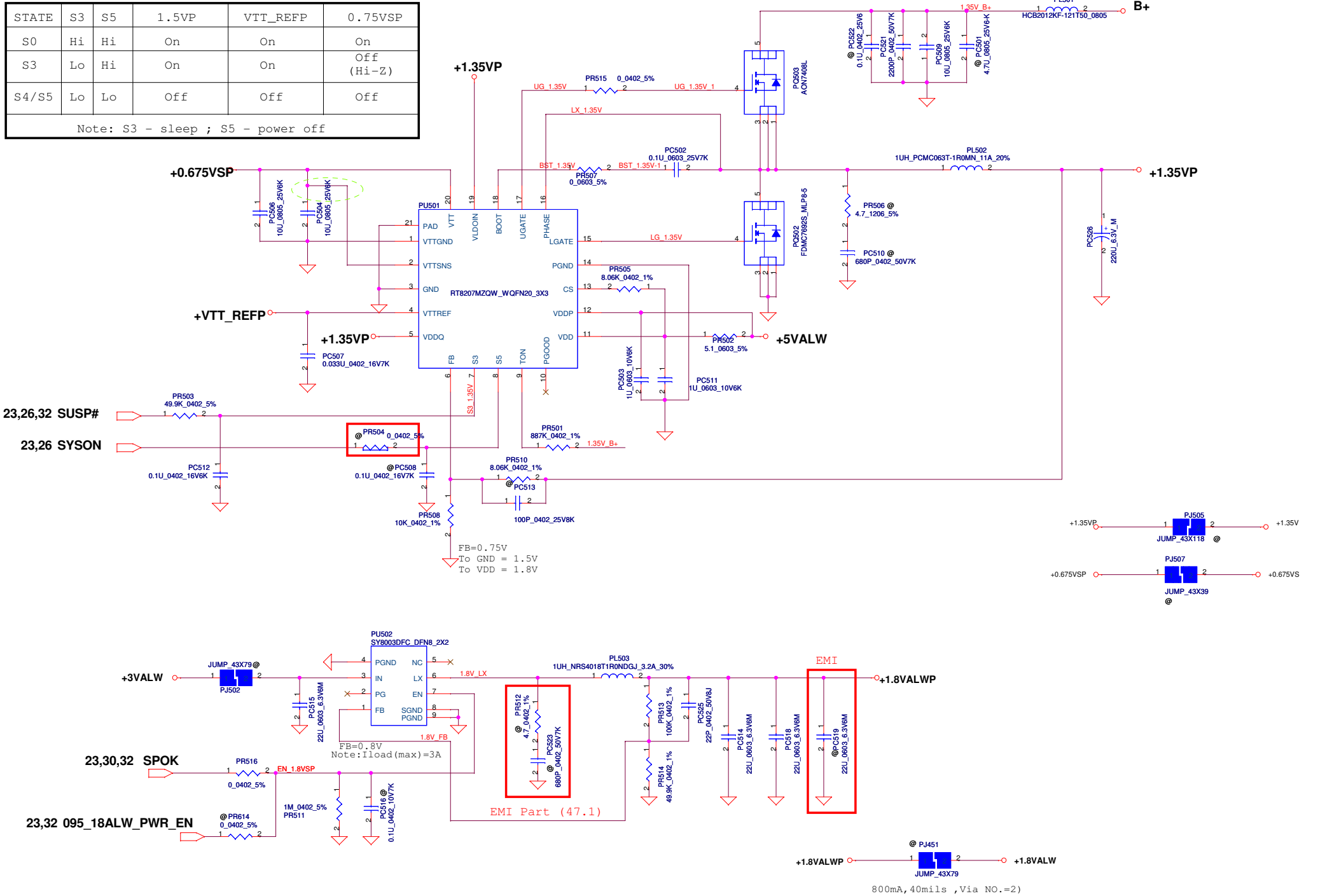
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Date: Monday, February 04, 2013				Sheet 28	of 40



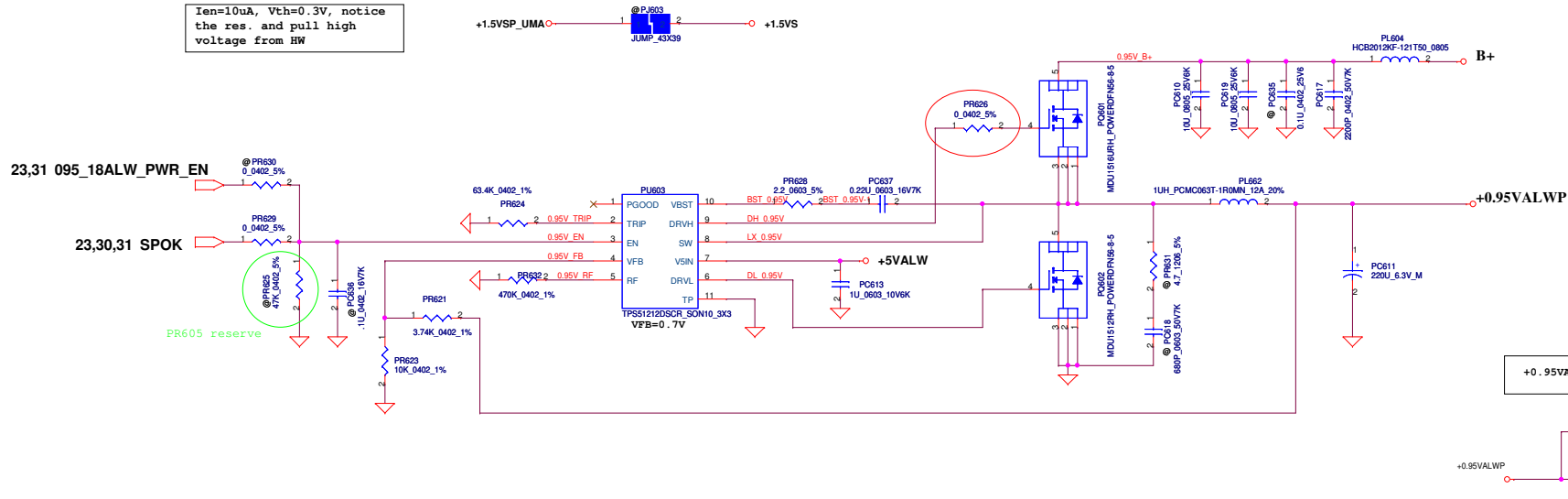
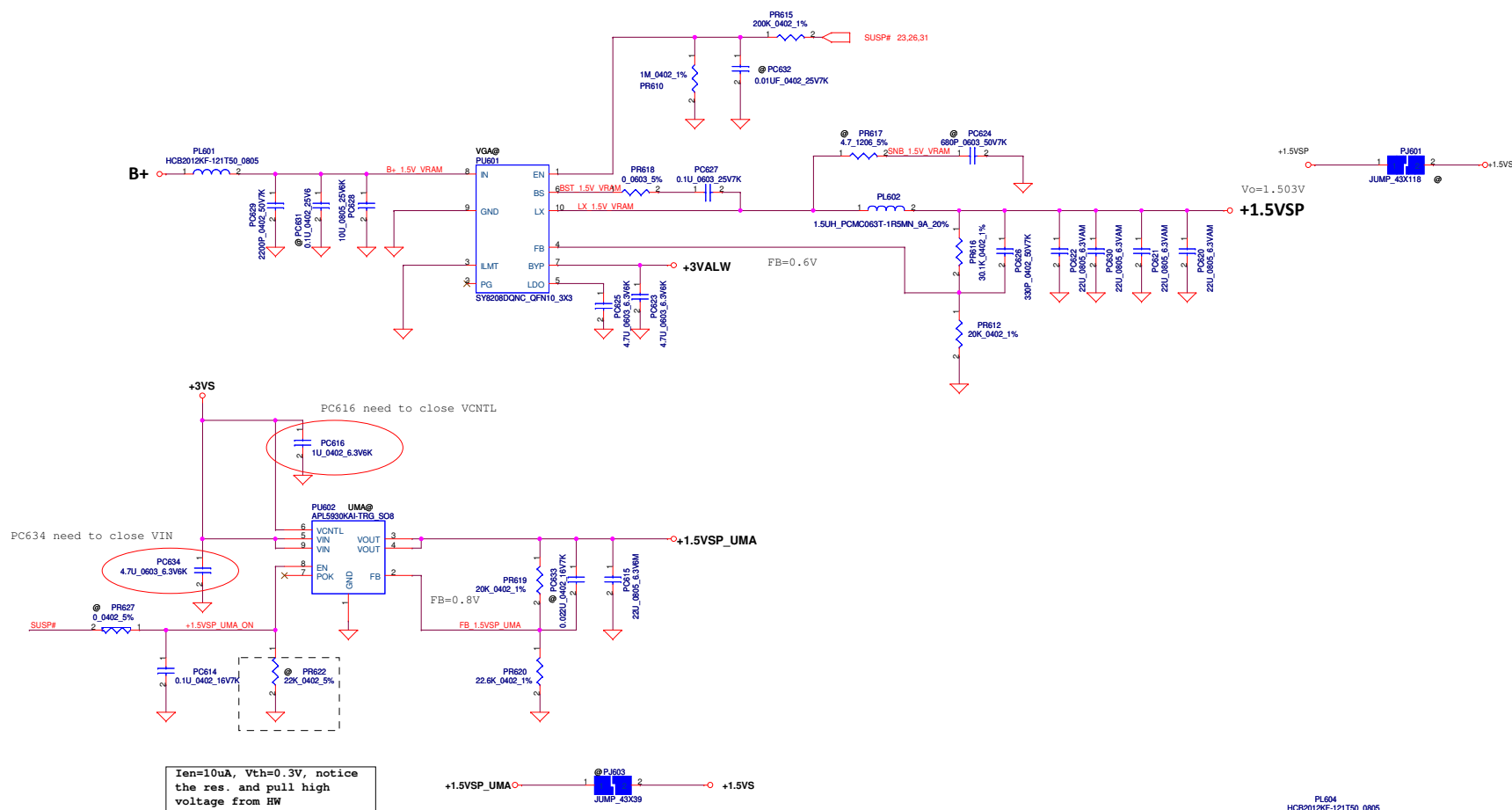
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STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

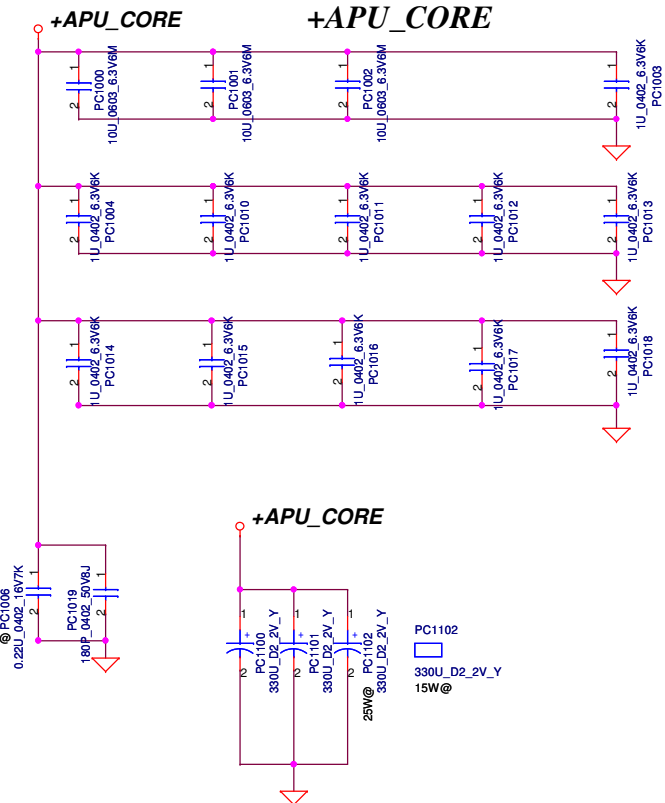
Note: S3 - sleep ; S5 - power off



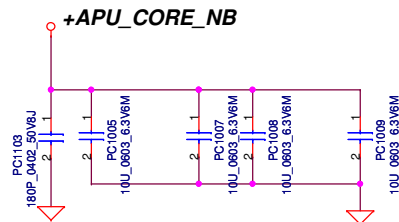
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Size	Custom	Document Number	C38-AMD KABINI Schematic	Rev	0.1
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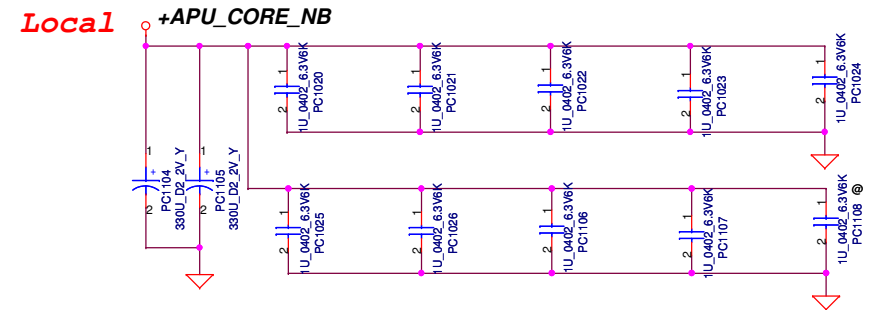
CPU_Core output CAP (Including MLCC) 36.4



+APU_CORE_NB



GFX output CAP (Including MLCC) 36.5



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Item	Modify List	PG#	Reason for change	Date	Phase
1					
2					
3					
4					
5					
6					
7					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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for HW

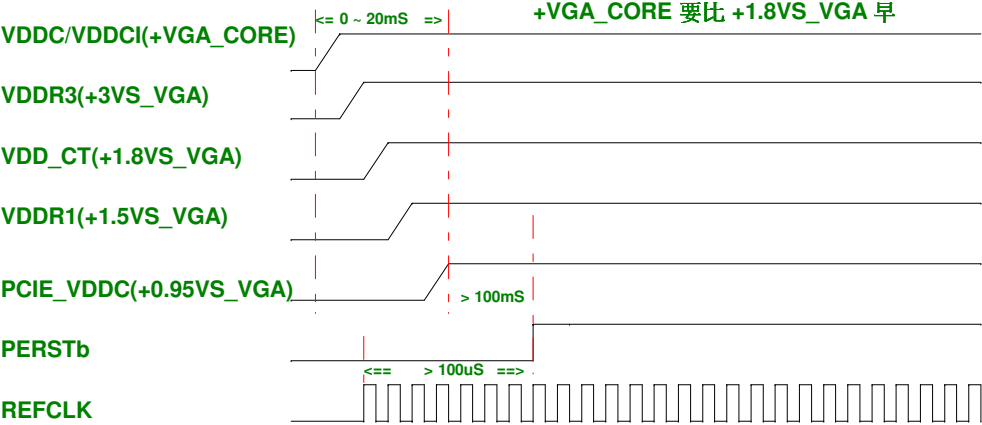
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				Size	Document Number	Rev
				Custom	C38-G series Chief River Schematic	0.1
Date:				Monday, February 04, 2013	Sheet	37 of 40

Power-Up/Down Sequence

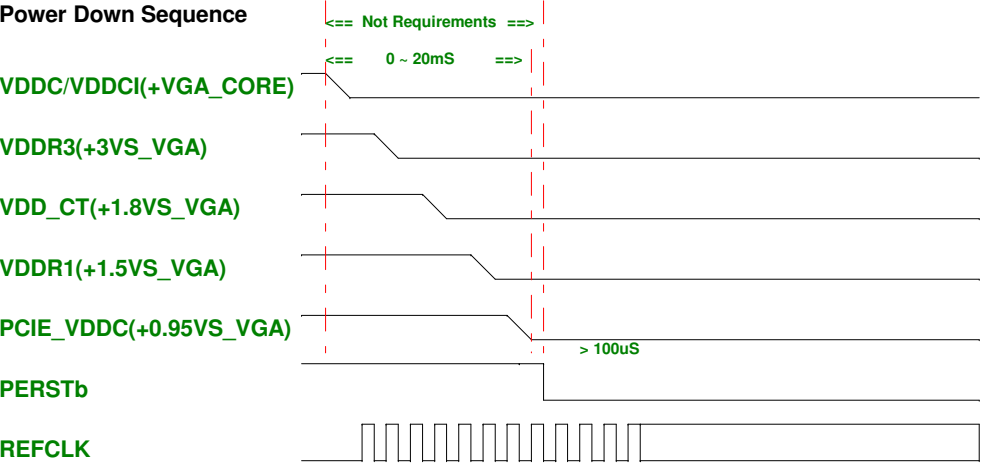
"Sun" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

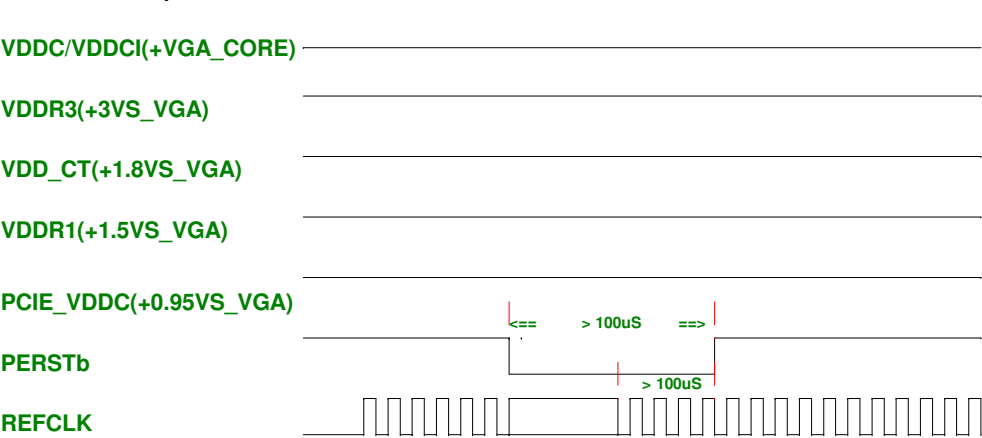
Cold Boot Sequence



Power Down Sequence

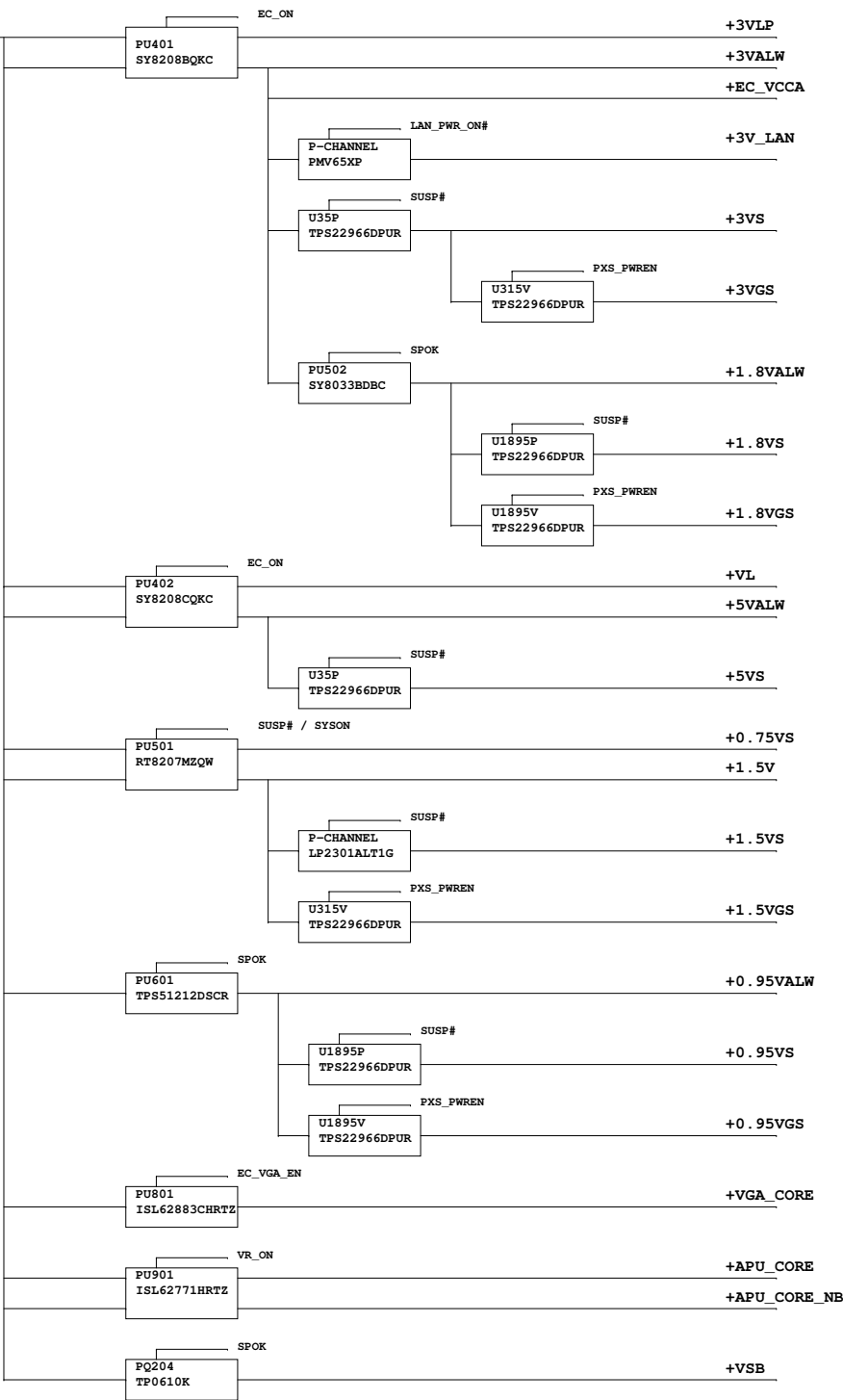


Warm Boot Sequence

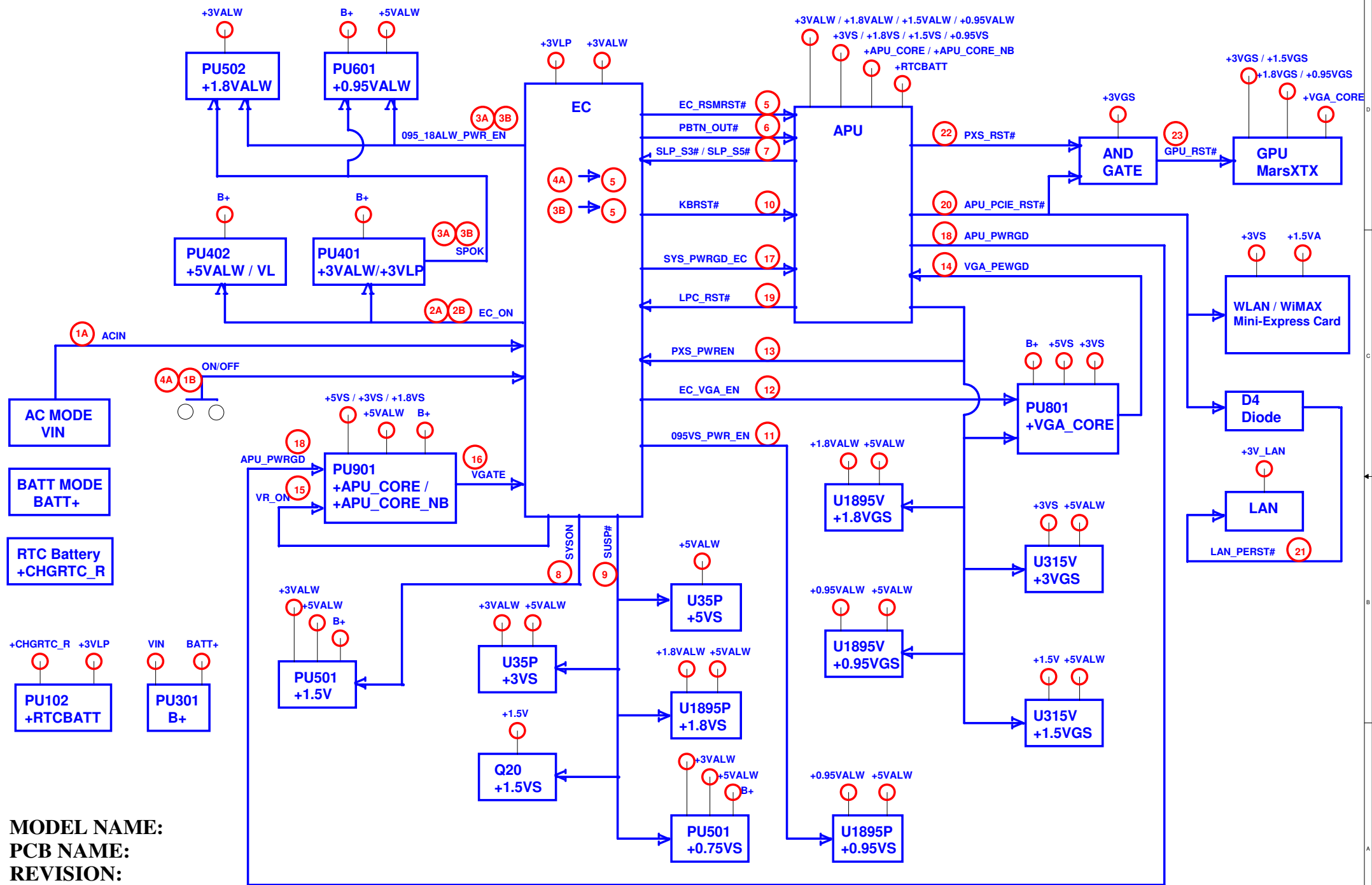


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				Size		
				Document Number		
				Rev		0.1
				LA-A331P		
				Date: Monday, February 04, 2013		Sheet 39 of 40



MODEL NAME:
 PCB NAME:
 REVISION:
 DATE: 2011/11/23

COMPAL CONFIDENTIAL

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				1	0.1

Compal Electronics, Inc.

Power sequence